## REMARKS

This application has been reviewed in light of the Office Action dated December 15, 2003. Claims 17 and 18 are pending in this application, with Claim 17 being in independent form. Favorable reconsideration is requested.

The Office Action objected to the drawings and specification, stating that for Figure 2, "MUX 9" should be replaced with --DEMUX 9--, and that the specification should be amended to reflect this change. Applicant attaches hereto a Replacement Sheet for Figure 2 making this change and, as shown above, has amended the specification accordingly. Consequently, Applicant hereby requests that these objections be withdrawn.

The Office Action rejected Claims 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,900,857 (Kuwata et al.) in view of U.S. Patent No. 4,745,485 (Iwasaki). Applicant respectfully traverses this rejection.

Applicant submits that independent Claim 17, together with Claim 18 depending therefrom, are patentably distinct from the proposed combination of the cited prior art at least for the following reasons.

The aspect of the present invention set forth in Claim 17 is a memory controller comprising a converter section, a first FIFO (first-in-first-out) section, a frame memory section, and a second FIFO section. The converter section performs serial/parallel conversion of image data of "a" bit width inputted into image data of "a" x "2n"-bit width, where "a" is a natural number representing a size of the inputted bit width and "n" is a natural number. The first FIFO section temporarily stores the image data of "a" x "2n"-bit width. The frame memory section stores image data of one frame and a second FIFO section temporarily stores image data read out from the frame memory section.

The image data is read out from the first FIFO section, written into the frame memory section, and read out from the frame memory section, at a rate that is half of a rate at which the image data is inputted into the first FIFO section. In addition, the first FIFO section is of a size suitable for storing image data, so that, within a period for inputting the image data into the first FIFO section to FULL capacity, writing the image data into the frame memory section, a plural times of reading the image data from the frame memory section, and executing a command of the frame memory section are conducted.

Among the notable feature of Claim 17 is that the image data is read out from the frame memory in half the rate of writing into the frame memory.

Kuwata et al., as understood by Applicant, relates to a method of driving a liquid crystal display device and a driving circuit for the liquid crystal display device. The Examiner pointed out in the Office Action at page 3 that Kuwata discloses in Fig. 1 and at column 11, lines 44-67, that an image data is read out from a frame memory 3 at a rate that is half of a rate at which the image data R, G, and B (6) is inputted into the first FIFO 2. Applicant submits, however, that this section of the Kuwata specification merely discusses that one frame of data including one bit per each of R, G, and B stored in DRAM 3 is read out by 120 bits (3 x 40 pixels) per each one access and is transferred to FIFO 5. However, nothing in this section, or any other section of Kuwata, has been found that would teach or suggest a reading rate. That is, Kuwata merely discusses a bit width of data transfer between writing FIFO 2, DRAM 3, and reading FIFO 5. Moreover, Kuwata discusses a driving method of a liquid crystal display device by a method of selecting simultaneously a plurality of lines. Accordingly, in order to scan a plural times using the same image data, it is necessary that a rate of reading from a memory be higher than a rate of writing therein

(column 6, lines 44-48). Accordingly, Applicant submits that nothing in Kuwata has been found that would teach or suggest that the image data is read out from the frame memory 3 at a rate that is half of the writing speed, as recited in Claim 17.

Iwasaki, as understood by Applicant, relates to a picture display device. In Iwasaki, an image data controlling method of a liquid crystal display apparatus is divided into upper and lower halves of display areas, reading from and writing into two memories corresponding respectively to the upper and lower halves of the display areas are conducted alternatively, and information for the divided upper and lower display area image information are read out alternatively. In Iwasaki, both of the two frame memories 4 and 5 are necessary to store the image data of one frame. Accordingly, the dividing is conducted merely for the purpose of discriminating a memory address (see Fig. 1). Writing into the image memory may be conducted in a manner of sequentially writing from the upper display area frame memory (see Fig. 2), or in a manner of writing the upper and lower display area frame memories 4 and 5 alternatively (see Fig. 8). Reading from may be conducted from the upper and lower display area frame memories 4 and 5, alternatively.

In Iwasaki, reading and writing rates are the same, and are merely described as two series of data addresses, as shown in Figs. 2, 5, and 8. That is, referring to Fig. 2, the writing is executed at "L" in (f) READ WRITE TIMING SIGNAL (R/W) while the reading is executed at "H" in (f) READ WRITE TIMING. In an image data transfer from the frame memories 4 and 5, an upper display area is latched by a latch circuit 6, and is transferred to a driver 9 together with the image information of the lower display area.

Accordingly, a rate of transferring the image signal to the driver 9 is a half of a rate of writing into the frame memory. Applicant submits, however, that nothing has been found in Iwasaki that would teach or suggest that the image data is read out from the frame memory 3 in half the rate of writing into the frame memory, as recited in Claim 17.

Accordingly, Applicant submits that at least for these reasons, Claim 17 is patentable over these two patents, taken separately or in any proper combination.

Claim 18 depends from Claim 17 and, therefore, is submitted to be patentable for at least the same reasons. Since Claim 18 is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

This Amendment After Final Action is believed to place this application in condition for allowance and, therefore, its entry is believed proper under 37 C.F.R. § 1.116. Accordingly, entry of this Amendment After Final Action, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested. Should the Examiner believe that issues remain outstanding, it is respectfully requested that the Examiner contact Applicants' undersigned attorney in an effort to resolve such issues and advance the case to issue.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and the allowance of the present application.

Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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